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LOADS	288338
STORE	496028
STORES	512563
BYPASS$3	0
BYPASS	142822
BYPASSA	1
BYPASSABL	1
BYPASSAED	1
BYPASSAGE	34
BYPASSCMD	9
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L27	l18 and load near8 store and bypass$3 near6 address$3	27	L27
L26	l18 and load near8 store and bypass$3 near6 address$3	27	L26
L25	l18 and load near8 store and bypass$3	156	L25
L24	l18 and load near8 store near8 address$3	280	L24
L23	l18 and load near8 store near8 (previous$3 or recent$3) near15 address$3	0	L23
L22	l18 and load near8 store near15 address$3	292	L22
L21	l18 and load near8 store	658	L21
L20	l1 and l18	0	L20
L19	l1 and L18	0	L19
L18	l16 not l1	2051	L18
L17	l1 and L16	1247	L17
L16	l1 or l2 or l3 or l4 or l6 or l7 or l8 or l9 or l10 or l11 or l12 or l13 or l14 or L15	3298	L16
L15	712/210	494	L15
L14	712/210	494	L14
L13	((712/245)!)!	718	L13
L12	(712/245)!	718	L12
L11	(((712/225)!)!)!	479	L11
L10	((712/225)!)!	479	L10
L9	(712/225)!	479	L9
L8	(((712/219)!)!)!	331	L8
L7	((712/219)!)!	331	L7
L6	(712/219)!	331	L6
L5	((812/210)!)!	0	L5
L4	((712/230)!)!	149	L4
L3	(712/230)!	149	L3
L2	(712/208)!	515	L2
L1	load near8 store near8 (previous$3 or after or before or recent$3 or last)	1247	L1

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1 **Performance comparison of load/store and symmetric instruction set architectures**
Alpert, D.; Averbuch, A.; Danieli, O.;
Computer Architecture, 1990. Proceedings. 17th Annual International Symposi
28-31 May 1990
Page(s): 172 -181

[Abstract] [PDF Full-Text (624 KB)] **IEEE CNF**

2 **Stream-interleaved pipelined RISC processor design for SIMD and MI system development**
Killeen, T.; Celenk, M.;
System Theory, 1993. Proceedings SSST '93., Twenty-Fifth Southeastern Sym
on , 7-9 March 1993
Page(s): 452 -456

[Abstract] [PDF Full-Text (468 KB)] **IEEE CNF**

3 **Predictive techniques for aggressive load speculation**
Reinman, G.; Calder, B.;
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE Interr
Symposium on , 30 Nov.-2 Dec. 1998
Page(s): 127 -137

[Abstract] [PDF Full-Text (152 KB)] **IEEE CNF**

4 **High performance issue oriented architecture**
Bhandarkar, D.; Orbits, D.; Witek, R.; Cardoza, W.; Cutler, D.;

Compcon Spring '90. 'Intellectual Leverage'. Digest of Papers. Thirty-Fifth IEEE Computer Society International Conference. , 26 Feb.-2 March 1990
Page(s): 153 -160

[Abstract] [PDF Full-Text (540 KB)] **IEEE CNF**

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5 **A VLSI implementation of the VAX vector architecture**
Fenwick, D.; Redford, J.; Stanley, T.; Williams, D.;
Compcon Spring '90. 'Intellectual Leverage'. Digest of Papers. Thirty-Fifth IEEE Computer Society International Conference. , 26 Feb.-2 March 1990
Page(s): 115 -119

[Abstract] [PDF Full-Text (256 KB)] **IEEE CNF**

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6 **Overview of the PIPE processor implementation**
Farrens, M.K.; Pleszkun, A.R.;
System Sciences, 1991. Proceedings of the Twenty-Fourth Annual Hawaii Inter Conference on , Volume: i , 8-11 Jan. 1991
Page(s): 433 -443 vol.1

[Abstract] [PDF Full-Text (860 KB)] **IEEE CNF**

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7 **A sea-of-gates-based, 10 MIPS 16-bit RISC processor testbed for fail applications**
Jurczyk, M.; Schwederski, T.;
Design Automation, 1993, with the European Event in ASIC Design. Proceedinç European Conference on , 22-25 Feb. 1993
Page(s): 536 -540

[Abstract] [PDF Full-Text (432 KB)] **IEEE CNF**

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8 **Fine-grain multi-thread processor architecture for massively parallel processing**
Kawano, T.; Kusakabe, S.; Taniguchi, R.-I.; Amamiya, M.;
High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symp(on , 22-25 Jan. 1995
Page(s): 308 -317

[Abstract] [PDF Full-Text (452 KB)] **IEEE CNF**

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9 **An object based data cache with conflict free concurrent access as sh memory for a parallel DSP**
Kneip, J.; Pirsch, P.;
VLSI Signal Processing, IX, 1996., [Workshop on] , 30 Oct.-1 Nov. 1996
Page(s): 25 -34

[Abstract] [PDF Full-Text (648 KB)] **IEEE CNF**

10 **Digital control for embedded applications**
Leach, R.;
Southcon/96. Conference Record , 25-27 June 1996
Page(s): 18 -22

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

11 **Efficient worst case timing analysis of data caching**
Sung-Kwan Kim; Sang Lyul Min; Rhan Ha;
Real-Time Technology and Applications Symposium, 1996. Proceedings., 1996
10-12 June 1996
Page(s): 230 -240

[Abstract] [PDF Full-Text (908 KB)] **IEEE CNF**

12 **Improving the accuracy and performance of memory communicatio through renaming**
Tyson, G.S.; Austin, T.M.;
Microarchitecture, 1997. Proceedings. Thirtieth Annual IEEE/ACM International Symposium on , 1-3 Dec. 1997
Page(s): 218 -227

[Abstract] [PDF Full-Text (1240 KB)] **IEEE CNF**

13 **RCRS: a framework for loop scheduling with limited number of regis**
Kaisheng Wang; Ted Zhihong; Yu Edwin; Sha, H.-M.;
VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on , 19-21 Feb. 19
Page(s): 386 -391

[Abstract] [PDF Full-Text (200 KB)] **IEEE CNF**

14 **An enhanced floating point coprocessor for embedded signal proces and graphics applications**
Hinds, C.N.;
Signals, Systems, and Computers, 1999. Conference Record of the Thirty-Third Asilomar Conference on , Volume: 1 , 24-27 Oct. 1999
Page(s): 147 -151 vol.1

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

15 **Issues in the design of store buffers in dynamically scheduled proce**
Bhargava, R.; John, L.K.;
Performance Analysis of Systems and Software, 2000. ISPASS. 2000 IEEE International Symposium on , 24-25 April 2000
Page(s): 76 -87

[Abstract] [PDF Full-Text (512 KB)] **IEEE CNF**

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Results:
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16 **Symbolic cache: fast memory access based on program syntax corre of loads and stores**
Qianrong Ma; Jih-Kwon Peir; Konrad Lai;
Computer Design, 2001. ICCD 2001. Proceedings. 2001 International Conferen
23-26 Sept. 2001
Page(s): 54 -61

[Abstract] [PDF Full-Text (648 KB)] **IEEE CNF**

17 **Design and implementation trade-offs in the Clipper C400 architectu**
Sachs, H.G.; McGhan, H.; Hanson, L.F.; Brookwood, N.A.;
Micro, IEEE , Volume: 11 Issue: 3 , June 1991
Page(s): 18 -21, 74-80

[Abstract] [PDF Full-Text (1548 KB)] **IEEE JNL**

18 **VIPER: a VLIW integer microprocessor**
Gray, J.; Naylor, A.; Abnous, A.; Bagherzadeh, N.;
Solid-State Circuits, IEEE Journal of , Volume: 28 Issue: 12 , Dec. 1993
Page(s): 1377 -1382

[Abstract] [PDF Full-Text (564 KB)] **IEEE JNL**

19 **A general purpose real time digital speech processor**
Mohiuddin, K.; Narayan, S.; Chen, K.; Peterson, A.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on IC
'81 , Volume: 6 , Apr 1981

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[Abstract] [PDF Full-Text (60 KB)] **IEEE CNF**

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20 **A 120 MFLOPS CMOS floating-point processor**
Chai, P.; Chuk, T.; Fong, Y.H.; Hu, L.; Ng, K.; Prabhu, J.; Quek, A.; Samuels, , Yeun, J.;
Custom Integrated Circuits Conference, 1991., Proceedings of the IEEE 1991 , May 1991
Page(s): 15.1/1 -15.1/4

[Abstract] [PDF Full-Text (256 KB)] **IEEE CNF**

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21 **A two-chip CMOS 64 b mainframe processor chipset**
Yamagishi, M.; Koide, K.; Ishiyama, A.; Yamagiwa, A.; Hayashi, T.; Satou, Y.;
Custom Integrated Circuits Conference, 1991., Proceedings of the IEEE 1991 , May 1991
Page(s): 15.4/1 -15.4/4

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

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22 **A new amplifier and pipeline chip for silicon strip detector readout**
Horisberger, R.; Pitzl, D.;
Nuclear Science Symposium and Medical Imaging Conference, 1992., Conferen Record of the 1992 IEEE , 25-31 Oct. 1992
Page(s): 399 vol.1

[Abstract] [PDF Full-Text (36 KB)] **IEEE CNF**

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23 **A silicon vertex detector with pipelining front-end electronics for H1 HERA**
Gabathuler, K.; Horisberger, R.; Brogle, M.; Eichler, R.; Grab, C.; Pitzl, D.; Egl Steiner, S.; Truol, P.;
Nuclear Science Symposium and Medical Imaging Conference, 1992., Conferen Record of the 1992 IEEE , 25-31 Oct. 1992
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24 **A concurrent fault detection method for superscalar processors**
Pawlovsky, A.P.; Hanawa, M.;
Test Symposium, 1992. (ATS '92), Proceedings., First Asian (Cat. No.TH0458-(26-27 Nov. 1992
Page(s): 139 -144

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

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25 **FPA10-A 4 MFLOP floating point coprocessor for ARM**
Harrod, P.L.; Baum, A.J.; Biggs, J.P.; Howard, D.W.; Merritt, A.J.; Oldham, H.E D.J.; Watters, H.L.;
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993 , May 1993
Page(s): 4.3.1 -4.3.4

[Abstract] [PDF Full-Text (520 KB)] **IEEE CNF**

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26 **VIPER: A 25-MHz, 100-MIPS peak VLIW microprocessor**
Gray, J.; Naylor, A.; Abnous, A.; Bagherzadeh, N.;
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993 , May 1993
Page(s): 4.1.1 -4.1.5

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

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27 **Streamlining data cache access with fast address calculation**
Austin, T.M.; Pnevmatikatos, D.N.; Sohi, G.S.;
Computer Architecture, 1995. Proceedings. 22nd Annual International Sympos 22-24 June 1995
Page(s): 369 -380

[Abstract] [PDF Full-Text (1280 KB)] **IEEE CNF**

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28 **Architecture tradeoffs in in reduced instruction set computers: a cas study**
ElGebaly, H.; Abd-El-Barr, M.; McCrosky, C.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE I Rim Conference on , 17-19 May 1995
Page(s): 78 -81

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

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29 **Remote supervisory systems for power-electronics devices**
Dmowski, A.; Drazkiewicz, J.; Bugyi, R.;
Industrial Electronics, 1996. ISIE '96., Proceedings of the IEEE International Symposium on , Volume: 2 , 17-20 June 1996
Page(s): 1017 -1020 vol.2

[Abstract] [PDF Full-Text (668 KB)] **IEEE CNF**

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30 **A 250 MHz 5 W RISC microprocessor with on-chip L2 cache controlle**
Reed, P.; Alexander, M.; Alvarez, J.; Brauer, M.; Chai-Chin Chao; Croxton, C.; L.; Toan Le; Tai Ngo; Nicoletta, C.; Sanchez, H.; Taylor, S.; Vanderschaaf, N.; G.;
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC. IEEE International , 6-8 Feb. 1997
Page(s): 412 -413, 496

[Abstract] [PDF Full-Text (1348 KB)] **IEEE CNF**

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31 **A 533 MHz BiCMOS superscalar microprocessor**
Cohen, E.T.; Ballard, J.; Blomgren, J.; Brashears, C.S.; Moldenhauer, V.; Patti
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC. IEEE International , 6-8 Feb. 1997
Page(s): 164 -165, 448

[Abstract] [PDF Full-Text (1252 KB)] **IEEE CNF**

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32 **Datarol: a parallel machine architecture for fine-grain multithreadin**
Amamiya, M.; Tomiyasu, H.; Kusakabe, S.;
Massively Parallel Programming Models, 1997. Proceedings. Third Working Con on , 12-14 Nov. 1997
Page(s): 151 -162

[Abstract] [PDF Full-Text (1132 KB)] **IEEE CNF**

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33 **An x86 load/store unit with aggressive scheduling of load/store operations**
Hui-Yue Hwang; R-Ming Shiu; Jyh-Jiun Shann;
Parallel and Distributed Systems, 1998. Proceedings., 1998 International Conf on , 14-16 Dec. 1998
Page(s): 496 -503

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34 **Performance comparison of three alternatives of distributed multida systems: a global query perspective**
Chung-Min Chen; Wei Sun; Rishe, N.;

Performance, Computing and Communications, 1998. IPCCC '98., IEEE Interna
16-18 Feb. 1998
Page(s): 53 -59

[Abstract] [PDF Full-Text (692 KB)] **IEEE CNF**

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35 **Volume rendering using OpenGL and extensions**
Meissner, M.; Hoffmann, U.; Strasser, W.;
Visualization '99. Proceedings , 24-29 Oct. 1999
Page(s): 207 -526

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36 **Is SC+ILP=RC?**
Guiady, C.; Falsafi, B.; Vijaykumar, T.N.;
Computer Architecture, 1999. Proceedings of the 26th International Symposiur
2-4 May 1999
Page(s): 162 -171

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37 **Speculation techniques for improving load related instruction sched**
Yoaz, A.; Erez, M.; Ronen, R.; Jourdan, S.;
Computer Architecture, 1999. Proceedings of the 26th International Symposiur
2-4 May 1999
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[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

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38 **A 7^{th}-generation x86 microprocessor**
Hesley, S.; Andrade, V.; Burd, B.; Constant, G.; Correll, J.; Crowley, M.; Golde
Hopkins, N.; Islam, S.; Johnson, S.; Khondker, R.; Meyer, D.; Moench, J.; Part
Posey, R.; Weber, F.; Yong, J.;
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 199
International , 15-17 Feb. 1999
Page(s): 92 -93

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39 **A 40 mm^2 3 V 50 MHz 64 Mb 4-level cell NOR-type flash memory**
Campardo, G.; Micheloni, R.; Commodaro, S.; Yero, E.; Zammabio, M.; Mogno
Sacco, A.; Picca, M.; Manstleita, A.; Scotti, M.; Motta, I.; Golla, C.; Pierin, A.;
A.; Fulatsuya, T.; Makabe, R.; Kawai, S.; Kai, Y.; Shimizu, S.; Ohnakado, T.;
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[Abstract] [PDF Full-Text (282 KB)] **IEEE CNF**

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40 **The design and implementation of CalmIRISC32 floating point unit**
Cheol-Ho Jeong; Woo-Chan Park; Sang-Woo Kim; Tack-Don Han;
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Confe on , 28-30 Aug. 2000
Page(s): 327 -330

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

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41 **DStride: data-cache miss-address-based stride prefetching scheme f multimedia processors**
Hariprakash, G.; Achutharaman, R.; Omondi, A.R.;
Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceedings. Australasian , 29-30 Jan. 2001
Page(s): 62 -70

[Abstract] [PDF Full-Text (756 KB)] **IEEE CNF**

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42 **Scalability of scheduled data flow architecture (SDF) with register c**

Arul, J.M.; Kavi, K.M.;
Algorithms and Architectures for Parallel Processing, 2002. Proceedings. Fifth International Conference on , 23-25 Oct. 2002
Page(s): 214 -221

[Abstract] [PDF Full-Text (266 KB)] **IEEE CNF**

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43 **Cherry: Checkpointed early resource recycling in out-of-order microprocessors**
Martinez, J.F.; Renau, J.; Huang, M.C.; Prvulovic, M.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
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44 **A 32-bit microprocessor for Smalltalk**
Pendleton, J.M.; Kong, S.I.; Brown, E.W.; Dunlap, F.; Marino, C.; Ungar, D.M.; Patterson, D.A.; Hodges, D.A.;
Solid-State Circuits, IEEE Journal of , Volume: 21 Issue: 5 , Oct 1986
Page(s): 741 -749

[Abstract] [PDF Full-Text (1400 KB)] **IEEE JNL**

45 **A 9-ns HIT-delay 32-kbyte cache macro for high-speed RISC**
Nogami, K.; Sakurai, T.; Sawada, K.; Sakaue, K.; Miyazawa, Y.; Tanaka, S.; H Y.; Katoh, K.; Takayanagi, T.; Shirotori, T.; Itoh, Y.; Uchida, M.; Iizuka, T.;
Solid-State Circuits, IEEE Journal of , Volume: 25 Issue: 1 , Feb. 1990
Page(s): 100 -108

[Abstract] [PDF Full-Text (736 KB)] **IEEE JNL**

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46 **A 320 MFLOPS CMOS floating-point processing unit for superscalar processors**
Ide, N.; Fukuhisa, H.; Kondo, Y.; Yoshida, T.; Nagamatsu, M.; Junji, M.; Yama. Ueno, K.;
Solid-State Circuits, IEEE Journal of , Volume: 28 Issue: 3 , March 1993
Page(s): 352 -361

[Abstract] [PDF Full-Text (960 KB)] **IEEE JNL**

47 **Access graphs: a model for investigating memory consistency**
Linder, D.H.; Harden, J.C.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 5 Issue: 1 , J 1994
Page(s): 39 -52

[Abstract] [PDF Full-Text (1304 KB)] **IEEE JNL**

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☐ 1. Document ID: US 6157981 A

L3: Entry 1 of 12 File: USPT Dec 5, 2000

US-PAT-NO: 6157981
DOCUMENT-IDENTIFIER: US 6157981 A

TITLE: Real time invariant behavior cache

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 5983336 A

L3: Entry 2 of 12 File: USPT Nov 9, 1999

US-PAT-NO: 5983336
DOCUMENT-IDENTIFIER: US 5983336 A

TITLE: Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 5923871 A

L3: Entry 3 of 12 File: USPT Jul 13, 1999

US-PAT-NO: 5923871
DOCUMENT-IDENTIFIER: US 5923871 A

TITLE: Multifunctional execution unit having independently operable adder and multiplier

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 5889985 A

L3: Entry 4 of 12 File: USPT Mar 30, 1999

US-PAT-NO: 5889985
DOCUMENT-IDENTIFIER: US 5889985 A

TITLE: Array prefetch apparatus and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
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☐ 5. Document ID: US 5408626 A

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US-PAT-NO: 5408626
DOCUMENT-IDENTIFIER: US 5408626 A

TITLE: One clock address pipelining in segmentation unit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 6. Document ID: US 5226129 A

L3: Entry 6 of 12 File: USPT Jul 6, 1993

US-PAT-NO: 5226129
DOCUMENT-IDENTIFIER: US 5226129 A

TITLE: Program counter and indirect address calculation system which concurrently performs updating of a program counter and generation of an effective address

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 7. Document ID: US 5136696 A

L3: Entry 7 of 12 File: USPT Aug 4, 1992

US-PAT-NO: 5136696
DOCUMENT-IDENTIFIER: US 5136696 A

TITLE: High-performance pipelined central processor for predicting the occurrence of executing single-cycle instructions and multicycle instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 8. Document ID: US 4342080 A

L3: Entry 8 of 12 File: USPT Jul 27, 1982

US-PAT-NO: 4342080
DOCUMENT-IDENTIFIER: US 4342080 A

TITLE: Computer with microcode generator system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 9. Document ID: US 4302809 A

L3: Entry 9 of 12 File: USPT Nov 24, 1981

US-PAT-NO: 4302809
DOCUMENT-IDENTIFIER: US 4302809 A

TITLE: External data store memory device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 10. Document ID: US 4218757 A

L3: Entry 10 of 12 File: USPT Aug 19, 1980

US-PAT-NO: 4218757
DOCUMENT-IDENTIFIER: US 4218757 A

TITLE: Device for automatic modification of ROM contents by a system selected variable

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 11. Document ID: US 4138738 A

L3: Entry 11 of 12 File: USPT Feb 6, 1979

US-PAT-NO: 4138738
DOCUMENT-IDENTIFIER: US 4138738 A

TITLE: Self-contained relocatable memory subsystem

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 12. Document ID: US 3976978 A

L3: Entry 12 of 12 File: USPT Aug 24, 1976

US-PAT-NO: 3976978
DOCUMENT-IDENTIFIER: US 3976978 A

TITLE: Method of generating addresses to a paged memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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Term	Documents
EFFECTIVE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1396775
EFFECTIVES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	53
ADDRESS$3	0
ADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	455570
ADDRESSA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	15
ADDRESSAB.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
ADDRESSABE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	7
ADDRESSABL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ADDRESSACK.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
ADDRESSAGE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ADDRESSAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
(EFFECTIVE NEAR3 ADDRESS$3 NEAR5 INSTRUCTION$ NEAR8 (RELATIVE OR RELATIONSHIP$) NEAR5 ADDRESS$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	12

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6360314 B1

L3: Entry 1 of 2 File: USPT Mar 19, 2002

US-PAT-NO: 6360314
DOCUMENT-IDENTIFIER: US 6360314 B1

TITLE: Data cache having store queue bypass for out-of-order instruction execution and method for same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 5751946 A

L3: Entry 2 of 2 File: USPT May 12, 1998

US-PAT-NO: 5751946
DOCUMENT-IDENTIFIER: US 5751946 A

TITLE: Method and system for detecting bypass error conditions in a load/store unit of a superscalar processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

Generate Collection | Print

Term	Documents
LOAD	1283606
LOADS	288248
STORE	495800
STORES	511984
ADDRESS	530668
ADDRESSES	219785
COMPAR$5	0
COMPAR	4018
COMPARA	4497
COMPARAATOR	5
COMPARABALE	5
(LOAD NEAR5 STORE NEAR5 ADDRESS NEAR4 COMPAR$5 NEAR10 BYPASS$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	2

There are more results than shown above. Click here to view the entire set.

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Search Results - Record(s) 1 through 20 of 27 returned.

☐ 1. Document ID: US 6499098 B1

L27: Entry 1 of 27 File: USPT Dec 24, 2002

US-PAT-NO: 6499098
DOCUMENT-IDENTIFIER: US 6499098 B1

TITLE: Processor with instruction qualifiers to control MMU operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6430679 B1

L27: Entry 2 of 27 File: USPT Aug 6, 2002

US-PAT-NO: 6430679
DOCUMENT-IDENTIFIER: US 6430679 B1

TITLE: Pre-arbitrated bypasssing in a speculative execution microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 6314504 B1

L27: Entry 3 of 27 File: USPT Nov 6, 2001

US-PAT-NO: 6314504
DOCUMENT-IDENTIFIER: US 6314504 B1
**** See image for Certificate of Correction ****

TITLE: Multi-mode memory addressing using variable-length

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 6282633 B1

L27: Entry 4 of 27 File: USPT Aug 28, 2001

US-PAT-NO: 6282633
DOCUMENT-IDENTIFIER: US 6282633 B1

TITLE: High data density RISC processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 5. Document ID: US 6272619 B1

L27: Entry 5 of 27 File: USPT Aug 7, 2001

US-PAT-NO: 6272619
DOCUMENT-IDENTIFIER: US 6272619 B1

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 6. Document ID: US 6256720 B1

L27: Entry 6 of 27 File: USPT Jul 3, 2001

US-PAT-NO: 6256720
DOCUMENT-IDENTIFIER: US 6256720 B1

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 7. Document ID: US 6212629 B1

L27: Entry 7 of 27 File: USPT Apr 3, 2001

US-PAT-NO: 6212629
DOCUMENT-IDENTIFIER: US 6212629 B1

TITLE: Method and apparatus for executing string instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 8. Document ID: US 6189088 B1

L27: Entry 8 of 27 File: USPT Feb 13, 2001

US-PAT-NO: 6189088
DOCUMENT-IDENTIFIER: US 6189088 B1

TITLE: Forwarding stored dara fetched for out-of-order load/read operation to over-taken operation read-accessing same memory location

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 9. Document ID: US 6145074 A

L27: Entry 9 of 27 File: USPT Nov 7, 2000

US-PAT-NO: 6145074
DOCUMENT-IDENTIFIER: US 6145074 A
**** See image for Certificate of Correction ****

TITLE: Selecting register or previous instruction result bypass as source operand path based on bypass specifier field in succeeding instruction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 10. Document ID: US 6128723 A

L27: Entry 10 of 27 File: USPT Oct 3, 2000

US-PAT-NO: 6128723
DOCUMENT-IDENTIFIER: US 6128723 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 11. Document ID: US 6101594 A

L27: Entry 11 of 27 File: USPT Aug 8, 2000

US-PAT-NO: 6101594
DOCUMENT-IDENTIFIER: US 6101594 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 12. Document ID: US 6092181 A

L27: Entry 12 of 27 File: USPT Jul 18, 2000

US-PAT-NO: 6092181
DOCUMENT-IDENTIFIER: US 6092181 A
**** See image for Certificate of Correction ****

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 13. Document ID: US 6092177 A

L27: Entry 13 of 27 File: USPT Jul 18, 2000

US-PAT-NO: 6092177
DOCUMENT-IDENTIFIER: US 6092177 A

TITLE: Computer architecture capable of execution of general purpose multiple instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 14. Document ID: US 6038654 A

L27: Entry 14 of 27 File: USPT Mar 14, 2000

US-PAT-NO: 6038654
DOCUMENT-IDENTIFIER: US 6038654 A
**** See image for Certificate of Correction ****

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 15. Document ID: US 6016543 A

L27: Entry 15 of 27 File: USPT Jan 18, 2000

US-PAT-NO: 6016543
DOCUMENT-IDENTIFIER: US 6016543 A

TITLE: Microprocessor for controlling the conditional execution of instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 16. Document ID: US 6016532 A

L27: Entry 16 of 27 File: USPT Jan 18, 2000

US-PAT-NO: 6016532
DOCUMENT-IDENTIFIER: US 6016532 A

TITLE: Method for handling data cache misses using help instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 17. Document ID: US 5968163 A

L27: Entry 17 of 27 File: USPT Oct 19, 1999

US-PAT-NO: 5968163
DOCUMENT-IDENTIFIER: US 5968163 A

TITLE: Microcode scan unit for scanning microcode instructions using predecode data

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 18. Document ID: US 5909567 A

L27: Entry 18 of 27 File: USPT Jun 1, 1999

US-PAT-NO: 5909567
DOCUMENT-IDENTIFIER: US 5909567 A

TITLE: Apparatus and method for native mode processing in a RISC-based CISC processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 19. Document ID: US 5878252 A

L27: Entry 19 of 27 File: USPT Mar 2, 1999

US-PAT-NO: 5878252
DOCUMENT-IDENTIFIER: US 5878252 A

TITLE: Microprocessor configured to generate help instructions for performing data cache fills

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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☐ 20. Document ID: US 5852727 A

L27: Entry 20 of 27 File: USPT Dec 22, 1998

US-PAT-NO: 5852727
DOCUMENT-IDENTIFIER: US 5852727 A

TITLE: Instruction scanning unit for locating instructions via parallel scanning of start and end byte information

Generate Collection | Print

Term	Documents
LOAD	1284184
LOADS	288338
STORE	496028
STORES	512563
BYPASS$3	0
BYPASS	142822
BYPASSA	1
BYPASSABL	1
BYPASSAED	1
BYPASSAGE	34
BYPASSCMD	9
(L18 AND LOAD NEAR8 STORE AND BYPASS$3 NEAR6 ADDRESS$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	27

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Search Results - Record(s) 21 through 27 of 27 returned.

☐ 21. Document ID: US 5835968 A

L27: Entry 21 of 27 File: USPT Nov 10, 1998

US-PAT-NO: 5835968
DOCUMENT-IDENTIFIER: US 5835968 A

TITLE: Apparatus for providing memory and register operands concurrently to functional units

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 22. Document ID: US 5758195 A

L27: Entry 22 of 27 File: USPT May 26, 1998

US-PAT-NO: 5758195
DOCUMENT-IDENTIFIER: US 5758195 A

TITLE: Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 23. Document ID: US 5689720 A

L27: Entry 23 of 27 File: USPT Nov 18, 1997

US-PAT-NO: 5689720
DOCUMENT-IDENTIFIER: US 5689720 A

TITLE: High-performance superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 24. Document ID: US 5006980 A

L27: Entry 24 of 27 File: USPT Apr 9, 1991

US-PAT-NO: 5006980

DOCUMENT-IDENTIFIER: US 5006980 A
**** See image for Certificate of Correction ****

TITLE: Pipelined digital CPU with deadlock resolution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 25. Document ID: US 4875160 A

L27: Entry 25 of 27 File: USPT Oct 17, 1989

US-PAT-NO: 4875160
DOCUMENT-IDENTIFIER: US 4875160 A
**** See image for Certificate of Correction ****

TITLE: Method for implementing synchronous pipeline exception recovery

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 26. Document ID: US 4493027 A

L27: Entry 26 of 27 File: USPT Jan 8, 1985

US-PAT-NO: 4493027
DOCUMENT-IDENTIFIER: US 4493027 A

TITLE: Method of performing a call operation in a digital data processing system having microcode call and return operations

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 27. Document ID: US 4445177 A

L27: Entry 27 of 27 File: USPT Apr 24, 1984

US-PAT-NO: 4445177
DOCUMENT-IDENTIFIER: US 4445177 A

TITLE: Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

Generate Collection | Print

Term	Documents
LOAD	1284184
LOADS	288338
STORE	496028
STORES	512563
BYPASS$3	0
BYPASS	142822
BYPASSA	1
BYPASSABL	1
BYPASSAED	1
BYPASSAGE	34
BYPASSCMD	9
(L18 AND LOAD NEAR8 STORE AND BYPASS$3 NEAR6 ADDRESS$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	27

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